

## Low-cost set-top box decoder for H.264 and Microsoft VC1

Data Brief

### Features

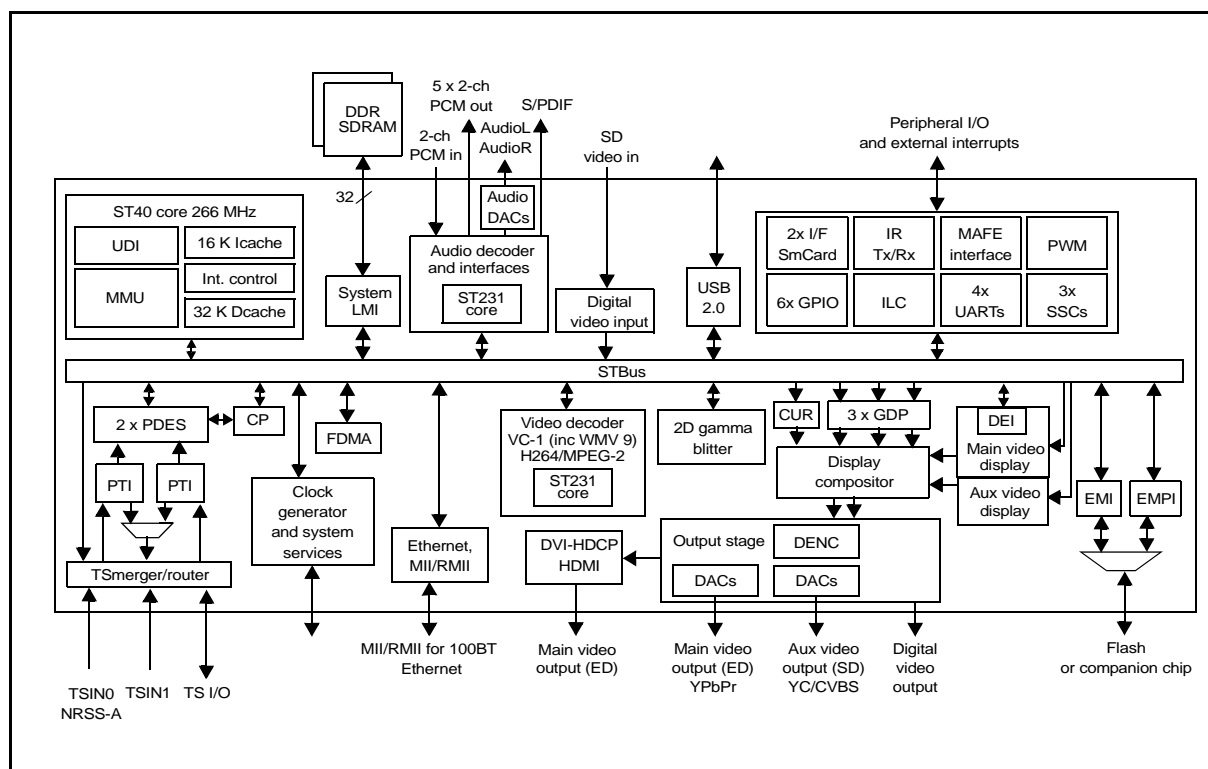
- Single-chip, video decoder including
  - Linux®, Windows® CE and OS21 compatible ST40 CPU core: 266 MHz
  - Transport filtering and descrambling
  - Video decoder: VC-1 (including WMV 9), H.264 (MPEG-4 part 10) and MPEG-2
  - SVP compliant
  - Windows Media™ DRM support
  - ST40 32-bit superscaler RISC CPU

### ■ Embedded interfaces

- USB 2.0 host controller/PHY interface
- DVI/HDMI™ output
- Digital audio and video auxiliary inputs
- Low-cost modem
- 100BT ethernet controller with integrated MAC and MII/RMII interface for external PHY

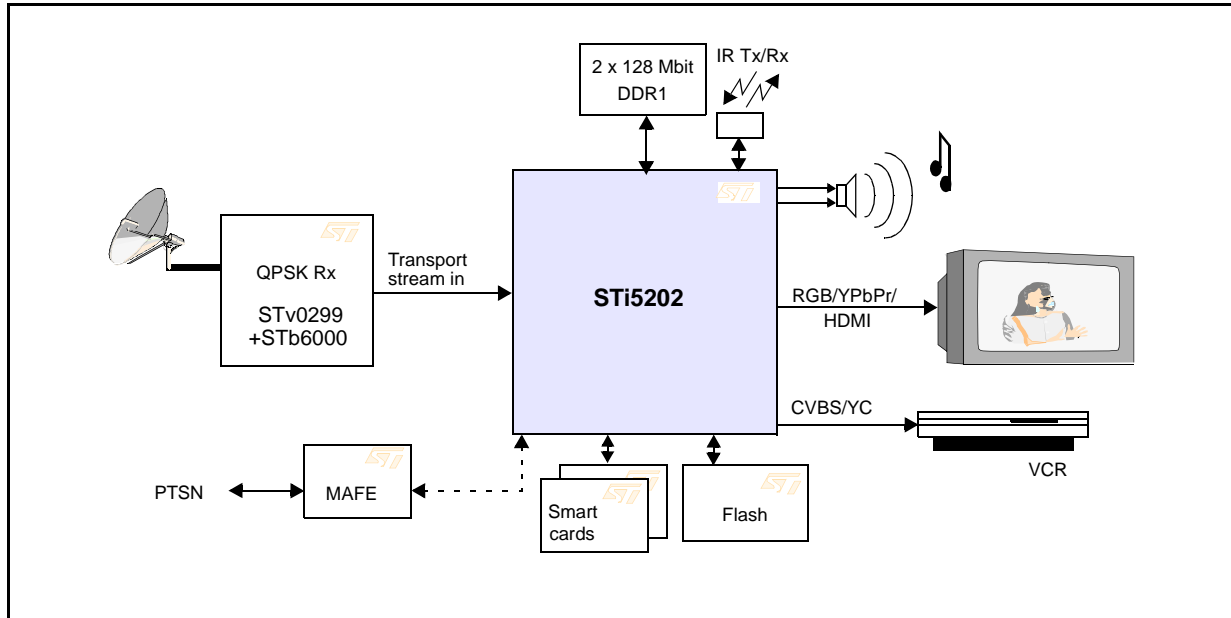
### Description

The STi5202 is a new generation, set-top box/DVD decoder chip, and provides very high performance for low-cost systems. STi5202 includes both VC1 and H.264 video decoders for new, low bit rate applications.

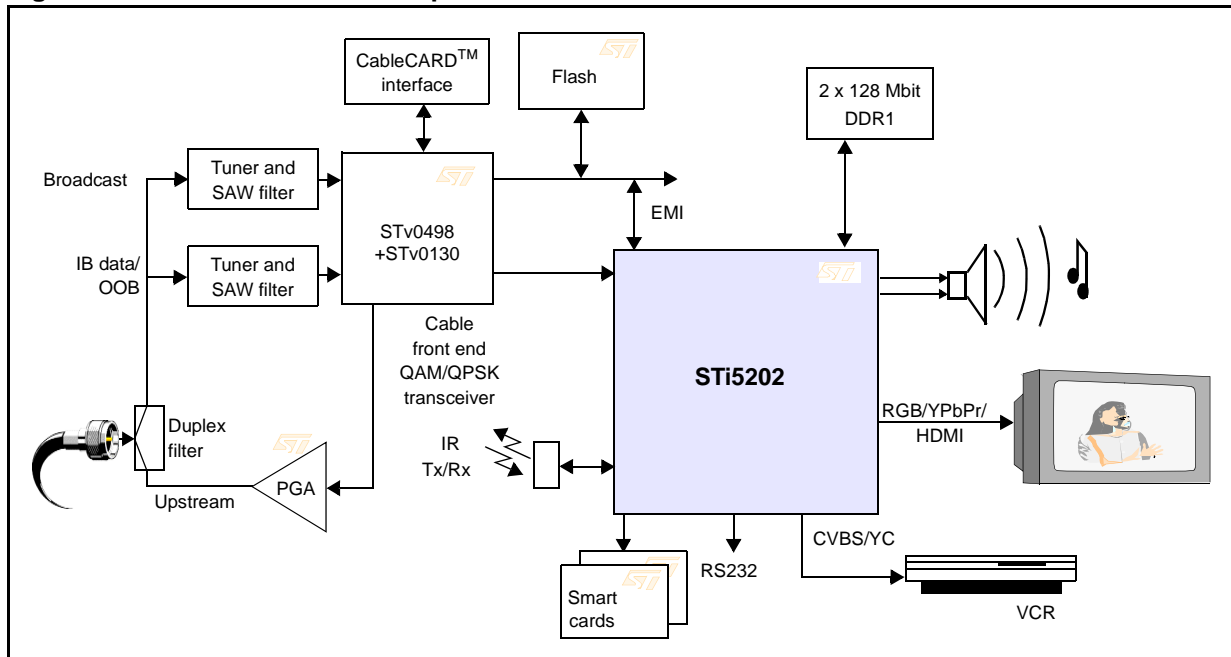


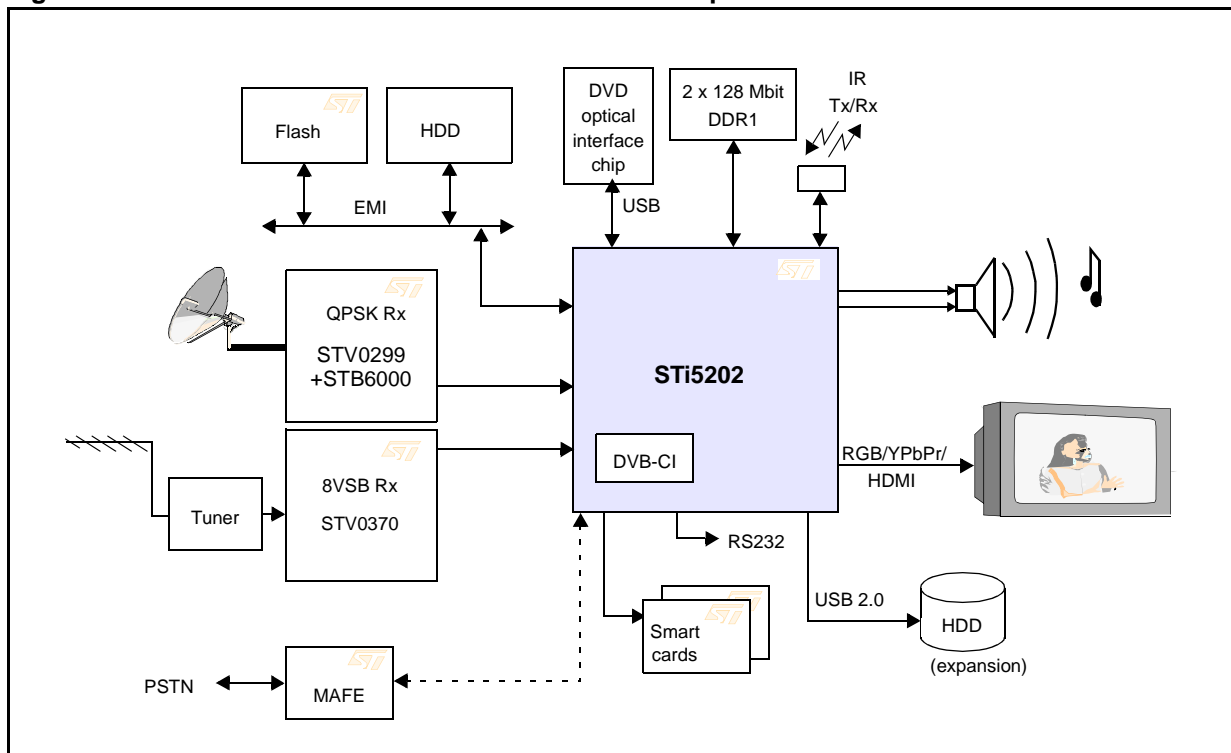
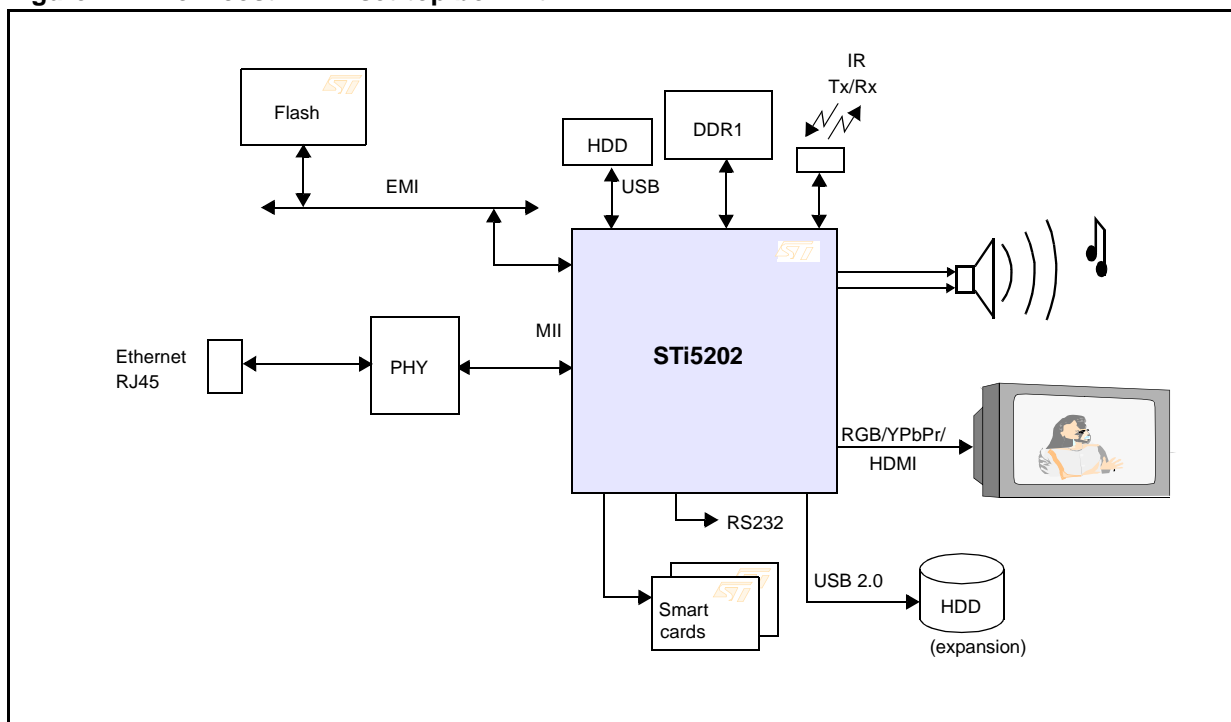
# 1 Typical applications

**Figure 1. Low-cost satellite set-top box**



**Figure 2. Low-cost cable set-top box with return channel**



**Figure 3. Low-cost dual satellite and terrestrial set-top box with HDD and DVD****Figure 4. Low-cost IP-TV set-top box with HDD**

## 1.1 Detailed features

The STi5202 is a single-chip, standard-definition video decoder including:

- Flexible audio decoder
- Windows Media™ DRM support
- Microsoft® VC-1, WMA9 and H.264 MPEG2 support
- Linux®, Windows® CE and OS21 compatible ST40 CPU core: 266 MHz
- Transport filtering and descrambling
- SVP compliant
- Graphics engine and dual display: standard and enhanced definition

The STi5202 also features the following embedded interfaces:

- USB 2.0 host controller/PHY interface
- DVI/HDMI™ output (optional)
- Low-cost modem
- 100BT ethernet controller with integrated MAC and MII/RMII interface for external PHY

The processor subsystem uses the ST40 32-bit superscaler RISC CPU and includes:

- 266 MHz, 2-way set associative 16-Kbyte ICache, 32-Kbyte DCache, MMU
- 5-stage pipeline, delayed branch support
- Floating point unit, matrix operation support
- Debug port, interrupt controller

The transport subsystem includes:

- TS merger/router
  - Merging of 3 external transport streams (2 serial/parallel inputs, 1 bidirectional interface)
  - Transport streams from memory support
  - NRSS-A module interface
- Programmable transport interfaces (PTIs)
  - Two programmable transport interfaces
  - Two transport stream demultiplexers: DVB, DIRECTV®, ATSC, ARIB, OpenCable, DCII
  - Integrated DES, AES, DVB and Multi2 descramblers
  - NDS random access scrambled stream protocol (RASP) compliant
  - NDS ICAM CA
  - Support for VGS, Passage

The video/graphics subsystem includes:

- Microsoft WMV 9/VC-1 MP@ML and AP@L1/H.264(MPEG-4 part 10) main and high profile level 3/MPEG-2 MP@ML video decoder
  - Advanced error concealment and trick mode support
  - Dual SD decoding
- SD digital video input
- Displays
  - One ED display multi format capable (480p/576p, 480i/576i)
    - analog ED output RGB or YPbPr
    - HDMI encoded output
  - One standard-definition display
    - analog SD output: YPbPr or YC and CVBS
- Gamma 2D graphics processor
  - Triple source 2D gamma blitter engine
  - Alpha blending and logical operations
  - Color space and format conversion
  - Fast color fill
  - Arbitrary resizing with high quality filters
  - Acceleration of direct drawing by CPU
- Gamma compositor and video processor
  - 7-channel mixer for enhanced definition output
  - Independent 2-channel mixer for SD output
  - 3 graphic display planes
  - High-quality video scaler
  - Motion and detail adaptive deinterlacer
  - Linear resizing and format conversions
  - Horizontal and vertical filtering
- Copy protection
  - HDMI/HDCP copy protection hardware
  - SVP compliant
  - Macrovision<sup>®</sup> copy protection for 480i, 480i, 576i, 576p outputs
  - DTCP-IP
  - AWG-based DCS analog copy protection

The audio subsystem includes:

- Digital audio decoder
  - Support for all the most popular audio standards including WMA-9, WMA-9 Pro, MPEG-1 layer I/II, MPEG-2 layer II, MPEG-2 AAC, MPEG-4 AAC LC 2-channel/5.1 channel MPEG-4 AAC+SBR 2-channel/5.1 channel, Dolby® Digital EX, Pro Logic® II, MLP™ and DTS®
  - PCM mixing with internal or external source and sample rate conversion
  - 6- to 2-channel downmixing
  - PCM audio input
  - Independent multichannel PCM output, S/PDIF output and analog output
- Stereo 24-bit audio DAC for analog output
- IEC958/IEC1937 digital audio output interface (S/PDIF)
- CSS/CPxM copy protection hardware

Available interfaces include:

- External memory interface (EMI)
  - 16-bit interface supporting ROM, flash, SFlash, SRAM, peripherals
  - Access in 5 banks
  - High speed synchronous mode for interconnecting two STi5202 devices
- External microprocessor interface (EMPI)
  - 32-bit MPX satellite, target-only interface
  - Synchronous operation at MPX clock speed, capable of 100 MHz
- Local memory interface (LMI)
  - Interface (1 x 32-bit) for DDR1 200-MHz (DDR400) memories, supports 128-, 256-, 512-Mbit, and 1-Gbit devices
- USB 2.0 host controller/PHY interface
- 100BT ethernet controller, MAC and MII/RMII

On-chip peripherals:

- 4 ASCs (UARTs) with Tx and Rx FIFOs, two of which can be used in smartcard interfaces
- 2 smartcard interfaces and clock generators (improved to reduce external circuitry)
- 3 SSCs for I<sup>2</sup>C/SPI master slaves interfaces
- Serial communications interface (SCIF)
- 2 PWM outputs
- Teletext serializer and DMA module
- 6 banks of general purpose I/O, 3.3 V tolerant
- SiLabs line-side (DAA) interface
- Modem analog front end (MAFE) interface
- Infrared transmitter/receiver supporting RC5, RC6 and RECS80 codes
- UHF remote receiver input interface
- Interrupt level controller and external interrupts, 3.3 V tolerant
- Low power/RTC/watchdog controller
- Integrated VCXO

- DiSEqC 2.0 interface
- PWM capture/compare functions
- Flexible multi-channel DMA

Services:

- JTAG/TAP interface, ST40 toolset support, ST231 toolset support

Package:

- 27 x 27 FPBGA, 620 balls.

## 2 Revision history

**Table 1. Document revision history**

Date	Revision	Changes
19-Oct-2007	1	Initial release.



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